What is Claimed is:

[c1] A varactor diode on a semiconductor substrate, comprising:

a well region of a first conductivity type in the substrate;

a plurality of isolation regions on upper portions of the well region;

a plurality of masking structures having first and second sides formed on the substrate between respective ones of said plurality of isolation regions;

a first plurality of diffusion regions of a second conductivity type, at least some of said plurality of diffusion regions abutting respective ones of said plurality of isolation regions; and

a second plurality of diffusion regions of said first conductivity type abutting portions of said first plurality of diffusion regions that do not abut respective ones of said plurality of isolation regions, said second plurality of diffusion regions extending below respective sides of respective ones of said plurality of masking structures, wherein respective ones of said second plurality of diffusion regions do not contact one another.

[c2] The diode of claim 1, further comprising a first electrical connection that interconnects said first plurality of diffusion regions.

[c3] The diode of claim 2, further comprising a second electrical connection to said well region.

[c4] The diode of claim 1, wherein said second plurality of diffusion regions have a dopant concentration greater than said first plurality of diffusion regions.

[c5] The diode of claim 4, wherein said second plurality of diffusion regions have a hyperabrupt doping profile.

[c6] The diode of claim 4, wherein said second plurality of diffusion regions have a dopant concentration of approximately.

[c7] A method of forming a varactor diode in a substrate, comprising:

forming a well region of a first conductivity type in the substrate;

forming a plurality of isolation regions on upper portions of the well

region;

forming a plurality of masking structures having first and second sides formed on the substrate between respective ones of said plurality of isolation regions;

forming a first plurality of diffusion regions of a second conductivity type, at least some of said plurality of diffusion regions abutting respective ones of said plurality of isolation regions; and

forming a second plurality of diffusion regions of said first conductivity type abutting portions of said first plurality of diffusion regions that do not abut respective ones of said plurality of isolation regions, said second plurality of diffusion regions extending below respective sides of respective ones of said plurality of masking structures, wherein respective ones of said second plurality of diffusion regions do not contact one another.

[c8] The method of claim 7, further comprising forming a first electrical connection that interconnects said first plurality of diffusion regions.

[c9] The method of claim 8, further comprising forming a second electrical connection to said well region.

[c10] The method of claim 7, wherein said step of forming said second plurality of diffusion regions comprises an angled implant.

[c11] The method of claim 10, wherein said angled implant is carried out at an angle of approximately.

[c12] The method of claim 11, wherein said second plurality of diffusion regions have a dopant concentration of approximately.

[c13] A varactor diode having a first electrode comprising a well region of a first conductivity type in a substrate, a second electrode comprising a first plurality of diffusion regions of a second conductivity type abutting isolation regions disposed in said well region, and a second plurality of diffusion regions of said first conductivity type extending laterally from portions of said first plurality of diffusion regions not adjacent said isolation regions and having a dopant

concentration greater than that of said first plurality of diffusion regions.

[c14] The varactor of claim 13, wherein said varactor has a Q of at least approximately 100 at a circuit operating frequency of approximately 2GHz and a tunability of at least approximately 2.5 to 3.5 in a range of applied voltage between approximately 0V to 3V, respectively.

[c15] A method of forming an integrated circuit on a semiconductor substrate, comprising:

forming first and second well regions of a first conductivity type in the substrate;

forming a plurality of isolation regions on upper portions of each of said well regions;

forming a plurality of conductive structures having first and second sides on each of said well regions, said structures comprising masking structures on said first well regions and gate electrodes on said second well regions;

masking said second well regions;

forming a first plurality of diffusion regions of a second conductivity type in said first well regions, at least some of said plurality of diffusion regions abutting respective ones of said plurality of isolation regions; and

forming a second plurality of diffusion regions of said first conductivity type in said first well regions abutting portions of said first plurality of diffusion regions that do not abut respective ones of said plurality of isolation regions, said second plurality of diffusion regions extending below respective sides of respective ones of said plurality of masking structures, wherein respective ones of said second plurality of diffusion regions do not contact one another.

[c16] The method of claim 15, wherein said substrate is selected from the group consisting of silicon, SiGe, and Group III-V semiconductors.

[c17] The method of claim 16, wherein said substrate is doped with an atom that increases strain and hence mobility of minority carriers.